TMC2330A

Coordinate Transformer

16 x 16 Bit, 50 MOPS

Features

- Rectangular-to-Polar or Polar-to-Rectangular conversion at guaranteed 50 MOPS pipelined throughput rate
- Polar data: 16-bit magnitude, 32-bit input/16-bit output phase
- 16-bit user selectable two's complement or sign-and-magnitude rectangular data formats
- Input register clock enables and asynchronous output enables simplify interfacing
- User-configurable phase accumulator for waveform synthesis and amplitude, frequency, or phase modulation
- Magnitude output data overflow flag (in Polar-to-Rectangular mode)
- Low power consumption CMOS process
- Single +5V power supply
- Available in a 120-pin plastic pin grid array package (PPGA) and 120-pin metric quad flatpack (MQFP)

Applications

- Scan conversion (phased array to raster)
- Vector magnitude estimation
- Range and bearing derivation
- Spectral analysis
- Digital waveform synthesis, including quadrature functions
- Digital modulation and demodulation

Description

The TMC2330A VLSI circuit converts bidirectionally between Cartesian (real and imaginary) and Polar (magnitude and phase) coordinates at up to 50 Mops (Million Operations Per Second).

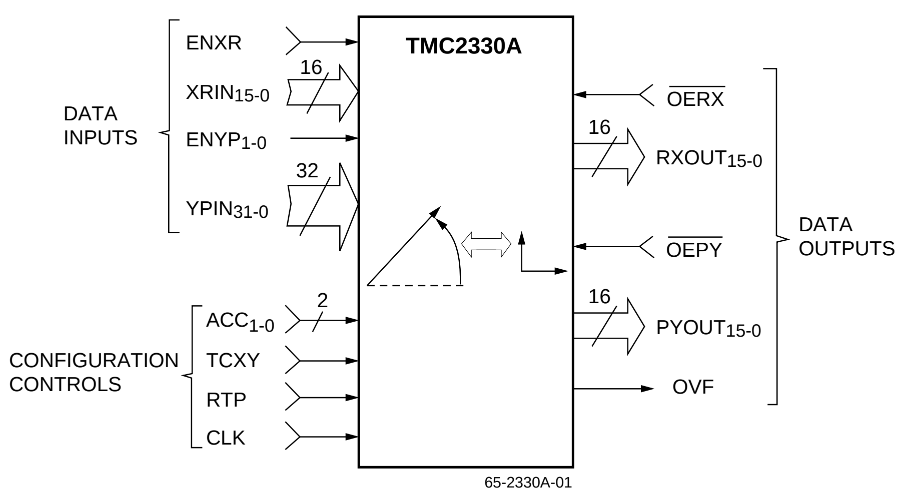
In its Rectangular-to-Polar mode, the TMC2330A can extract phase and magnitude information or backward "map" from a rectangular raster display to a radial (e.g., range-and-azimuth) data set.

The Polar-to-Rectangular mode executes direct digital waveform synthesis and modulation. The TMC2330A greatly simplifies real-time image-space conversion between the radially-generated image scan data found in radar, sonar, and medical imaging systems, and raster display formats.

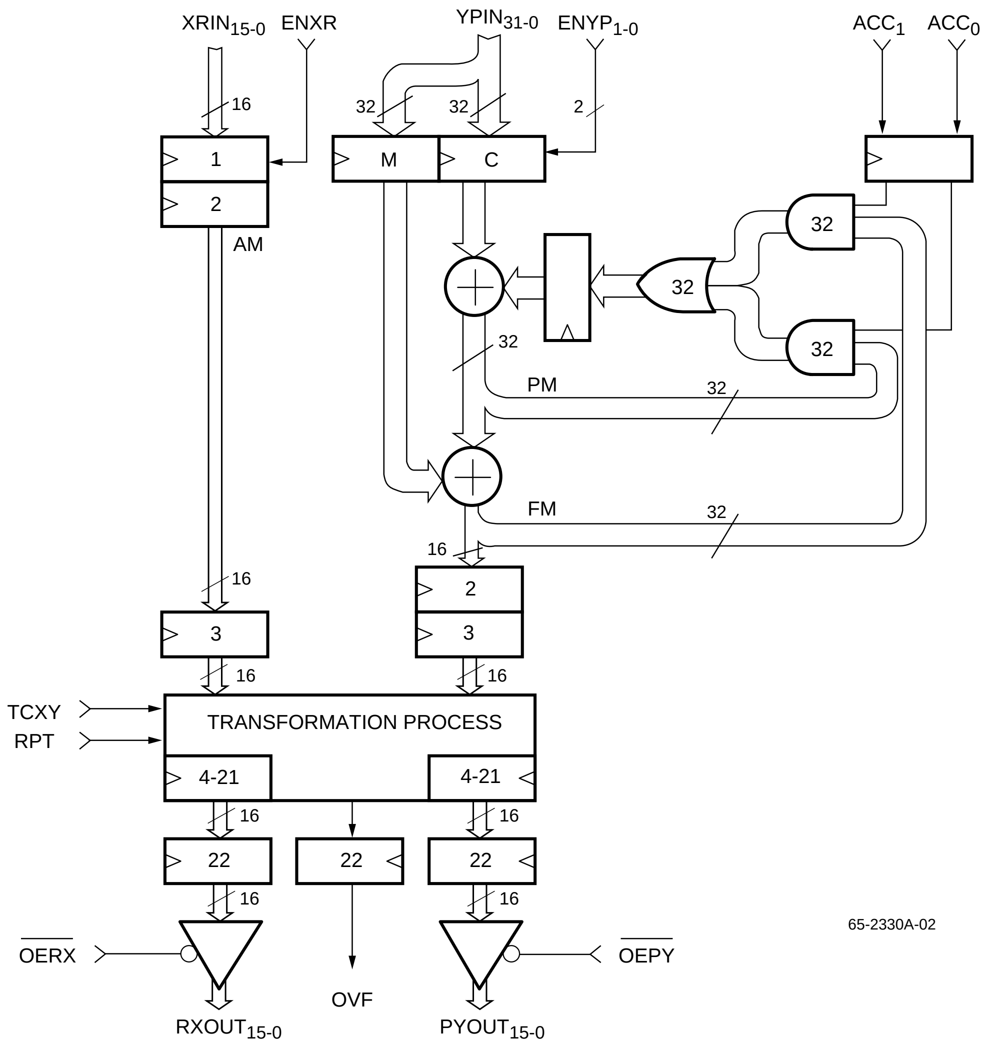
All input and output data ports are registered, and a new transformed data word pair is available at the output every clock cycle. The user-configurable phase accumulator structure, input clock enables, and asynchronous three-state output bus enables simplify interfacing. All signals are TTL compatible.

Fabricated in a submicron CMOS process, the TMC2330A operates at up to the 50 MHz maximum clock rate over the full commercial (0 to 70°C) temperature and supply voltage ranges, and is available in low-cost 120-pin plastic pin grid array and metric quad flatpack packages.

Logic Symbol



Block Diagram



Functional Description

The TMC2330A converts between Rectangular (Cartesian) and Polar (Phase and Magnitude) coordinate data word pairs. The user selects the numeric format and transformation to be performed (Rectangular-To-Polar or Polar-To-Rectangular), and the operation is performed on the data presented to the inputs on the next clock. The transformed result is then available at the outputs 22 clock cycles later, with new output data available every 20ns with a 50MHz clock. All input and output data ports are registered, with input clock enables and asynchronous high-impedance output enables to simplify connections to system buses.

When executing a Rectangular-To-Polar conversion, the input ports accept 16-bit Rectangular coordinate words, and the output ports generate 16-bit magnitude and 16-bit phase data. The user selects either two's complement or sign-and-magnitude Cartesian data format. Polar magnitude data are always in magnitude format only. Since the phase angle word is modulo 2π, it may be regarded as either unsigned or two's complement format (Tables 1 and 2).

In Polar-To-Rectangular mode, the input ports accept 16-bit Polar magnitude and 32-bit phase data, and the output ports produce 16-bit Rectangular data words. Again, the user selects between two's complement or sign-and-magnitude Cartesian data format.

Table 1. Data Input/Output Formats—Integer Format

			Bit #										
Port	**RTP**	**TCXY**	**31**	**30**	**29**	**…**	**16**	**15**	**14**	**…**	**0**	**Format**	
XRIN	0	X						2^{15}	2^{14}	…	2^{0}		U
XRIN	1	0						NS	2^{14}	…	2^{0}		S
XRIN	1	1						-2^{15}	2^{14}	…	2^{0}		T
YPIN	0	X	$\pm 2^{0}$	2^{-1}	2^{-2}	…	2^{-15}	2^{-16}	2^{-17}	…	2^{-31}	(xπ)T/U	
YPIN	1	0	NS	2^{14}	2^{13}	…	2^{0}						S
YPIN	1	1	-2^{15}	2^{14}	2^{13}		2^{0}						T
RXOUT	0	0						NS	2^{14}		2^{0}		S
RXOUT	0	1						-2^{15}	2^{14}		2^{0}		T
RXOUT	1	X						2^{15}	2^{14}		2^{0}		U
PYOUT	0	0						NS	2^{14}		2^{0}		S
PYOUT	0	1						-2^{15}	2^{14}		2^{0}		T
PYOUT	1	X						$\pm 2^{0}$	2^{-1}		2^{-15}	(xπ)T/U	

Table 2. Data Input/Output Formats—Fractional Format

			Bit #										
Port	**RTP**	**TCXY**	**31**	**30**	**29**	**…**	**16**	**15**	**14**	**…**	**0**	**Format**	
XRIN	0	X						2^{0}	2^{-1}	…	2^{-15}		U
XRIN	1	0						NS	2^{-1}	…	2^{-15}		S
XRIN	1	1						-2^{0}	2^{-1}	…	2^{-15}		T
YPIN	0	X	$\pm 2^{0}$	2^{-1}	2^{-2}	…	2^{-15}	2^{-16}	2^{-17}	…	2^{-31}	(xπ)T/U	
YPIN	1	0	NS	2^{-1}	2^{-2}	…	2^{-15}						S
YPIN	1	1	-2^{0}	2^{-1}	2^{-2}	…	2^{-15}						T
RXOUT	0	0						NS	2^{-1}	…	2^{-15}		S
RXOUT	0	1						-2^{0}	2^{-1}	…	2^{-15}		T
RXOUT	1	X						2^{0}	2^{-1}	…	2^{-15}		U
PYOUT	0	0						NS	2^{-1}	…	2^{-15}		S
PYOUT	0	1						-2^{0}	2^{-1}	…	2^{-15}		T
PYOUT	1	X						$\pm 2^{0}$	2^{-1}	…	2^{-15}	(xπ)T/U	

Notes:

1. -2^{15} denotes two's complement sign bit.
2. NS denotes negative sign, i.e., '1' negates the number.
3. $\pm 2^{0}$ denotes two's complement sign or highest magnitude bit – since phase angles are modulo 2π and phase accumulator is modulo 2^{32}, this bit may be regarded as +π or -π.
4. All phase angles are in terms of π radians, hence notation "xπ."
5. If A_{CC} = 00, YPIN(15-0) are "don't cares."
6. Formats:
   T = Two's Complement
   S = Signed Magnitude
   U = Unsigned

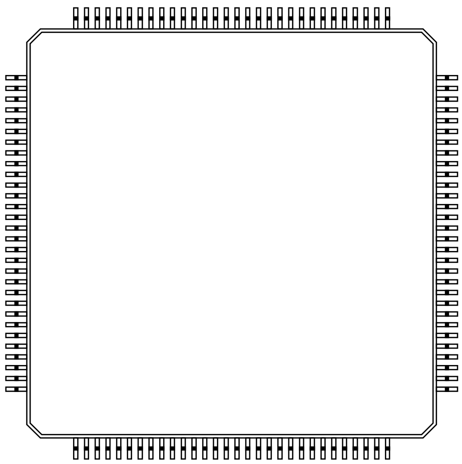
HEX	U	T	S
FFFF	65535	–1	-32767
…	…	…	…
8001	32769	-32767	-1
8000	32768	-32768	0
7FFF	32767	32767	32767
…	…	…	…
0001	1	1	1
0000	0	0	0

Static Control Inputs

The controls RTP and TCXY determine the transformation mode and the assumed numeric format of the Rectangular data. The user must exercise caution when changing either of these controls, as the new transformed results will not be seen at the outputs until the entire internal pipe (22 clocks) has been flushed. Thus, these controls are considered static.

Pin Assignments

120-Pin MQFP

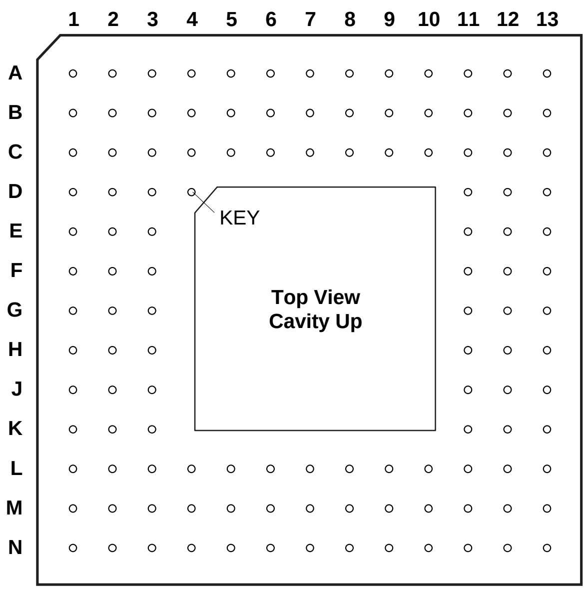


65-2330A-03

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VDD	31	GND	61	VDD	91	VDD
2	PYOUT4	32	YPIN9	62	XRIN1	92	RXOUT9
3	PYOUT3	33	YPIN10	63	XRIN2	93	RXOUT8
4	GND	34	VDD	64	GND	94	GND
5	PYOUT2	35	YPIN11	65	XRIN3	95	RXOUT7
6	PYOUT1	36	YPIN12	66	XRIN4	96	RXOUT6
7	PYOUT0	37	YPIN13	67	XRIN5	97	RXOUT5
8	VDD	38	YPIN14	68	GND	98	GND
9	$\overline{\text{OEPY}}$	39	YPIN15	69	XRIN6	99	RXOUT4
10	GND	40	YPIN16	70	XRIN7	100	RXOUT3
11	RTP	41	YPIN17	71	XRIN8	101	RXOUT2
12	CLK	42	VDD	72	XRIN9	102	VDD
13	GND	43	YPIN18	73	XRIN10	103	RXOUT1
14	TCXY	44	YPIN19	74	XRIN11	104	RXOUT0
15	ENPY	45	YPIN20	75	XRIN12	105	OVF
16	GND	46	GND	76	GND	106	GND
17	ENPY1	47	YPIN21	77	XRIN13	107	PYOUT15
18	ACC0	48	YPIN22	78	XRIN14	108	PYOUT14
19	ACC1	49	YPIN23	79	XRIN15	109	PYOUT13
20	VDD	50	VDD	80	VDD	110	VDD
21	YPIN0	51	YPIN24	81	$\overline{\text{OERX}}$	111	PYOUT12
22	YPIN1	52	YPIN25	82	GND	112	PYOUT11
23	YPIN2	53	YPIN26	83	RXOUT15	113	PYOUT10
24	YPIN3	54	YPIN27	84	VDD	114	GND
25	YPIN4	55	YPIN28	85	RXOUT14	115	PYOUT9
26	YPIN5	56	YPIN29	86	RXOUT13	116	PYOUT8
27	YPIN6	57	YPIN30	87	RXOUT12	117	PYOUT7
28	GND	58	YPIN31	88	GND	118	GND
29	YPIN7	59	ENXR	89	RXOUT11	119	PYOUT6
30	YPIN8	60	XRIN0	90	RXOUT10	120	PYOUT5

Pin Assignments (continued)

121-Pin PPGA



65-2330A-04

Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	PYOUT5	C5	GND	G11	GND	L10	YPIN31
A2	PYOUT7	C6	VDD	G12	XRIN12	L11	VDD
A3	PYOUT8	C7	GND	G13	RXIN13	L12	XRIN3
A4	PYOUT10	C8	VDD	H1	ACC0	L13	XRIN4
A5	PYOUT12	C9	GND	H2	ACC1	M1	YPIN6
A6	PYOUT14	C10	GND	H3	VDD	M2	YPIN9
A7	PYOUT15	C11	VDD	H11	XRIN9	M3	YPIN11
A8	RXOUT0	C12	RXOUT11	H12	XRIN10	M4	YPIN13
A9	RXOUT2	C13	RXOUT13	H13	XRIN11	M5	YPIN16
A10	RXOUT4	D1	$\overline{\text{OEPY}}$	J1	YPIN0	M6	YPIN18
A11	RXOUT6	D2	PYOUT0	J2	YPIN1	M7	YPIN20
A12	RXOUT8	D3	GND	J3	YPIN3	M8	YPIN23
A13	RXOUT10	D11	GND	J11	GND	M9	YPIN25
B1	PYOUT3	D12	RXOUT14	J12	XRIN7	M10	YPIN28
B2	PYOUT4	D13	RXOUT15	J13	XRIN8	M11	ENXR
B3	PYOUT6	E1	RTP	K1	YPIN2	M12	XRIN1
B4	PYOUT9	E2	GND	K2	YPIN4	M13	XRIN2
B5	PYOUT11	E3	VDD	K3	GND	N1	YPIN8
B6	PYOUT13	E11	VDD	K11	GND	N2	YPIN10
B7	OVF	E12	GND	K12	XRIN5	N3	YPIN12
B8	RXOUT1	E13	$\overline{\text{OERX}}$	K13	XRIN6	N4	YPIN15
B9	RXOUT3	F1	TCKY	L1	YPIN5	N5	YPIN17
B10	RXOUT5	F2	GND	L2	YPIN7	N6	YPIN19
B11	RXOUT7	F3	CLK	L3	GND	N7	YPIN21
B12	RXOUT9	F11	VDD	L4	VDD	N8	YPIN22
B13	RXOUT12	F12	RXIN15	L5	YPIN14	N9	YPIN24
C1	PYOUT1	F13	RXIN14	L6	VDD	N10	YPIN26
C2	PYOUT2	G1	ENPY1	L7	GND	N11	YPIN29
C3	VDD	G2	ENPY0	L8	VDD	N12	YPIN30
C4	GND	G3	GND	L9	YPIN27	N13	XRIN0

Pin Descriptions

Pin Name	Pin Number		Description
	PPGA	MQFP	
Power, Ground and Clock			
V_{DD}	1, 8, 20, 34, 42, 50, 61, 80, 84, 91, 102, 110	C3, E3, H3, L4, L6, L8, L11, F11, E11, C11, C8, C6	The TMC2330A operates from a single +5V supply. All power and ground pins must be connected.
GND	4, 10, 13, 16, 28, 31, 46, 64, 68, 76, 82, 88, 94, 98, 106, 114, 118	D3, E2, F2, G3, K3, L3, L7, K11, J11, G11, E12, D11, C10, C9, C7, C5, C4	Ground
CLK	12	F3	The TMC2330A operates from a single clock. All enabled registers are strobed on the rising edge of CLK, which is the reference for all timing specifications.

Pin Descriptions (continued)

Pin Name	Pin Number		Description
	PPGA	MQFP	
Inputs/Outputs			
$XRIN_{15-0}$	79, 78, 77, 75, 74, 73, 72, 71, 70, 69, 67, 66, 65, 63, 62, 60	F12, F13, G13, G12, H13, H12, H11, J13, J12, K13, K12, L13, L12, M13, M12, N13	$XRIN_{15-0}$ is the registered Cartesian X-coordinate or Polar Magnitude (Radius) 16-bit input data port. $XRIN_{15}$ is the MSB.
$YPIN_{31-0}$	58, 57, 56, 55, 54, 53, 52, 51, 49, 48, 47, 45, 44, 43, 41, 40, 39, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26, 25, 24, 23, 22, 21	L10, N12, N11, M10, L9, N10, M9, N9, M8, N8, N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, N2, M2, N1, L2, M1, L1, K2, J3, K1, J2, J1	$YPIN_{31-0}$ is the registered Cartesian Y-coordinate or Polar Phase angle 32-bit input data port. The input phase accumulators are fed through this port in conjunction with the input enable select $ENYP_{1,0}$. When RTP is HIGH (Rectangular-To-Polar), the input accumulators are normally not used. The 16 MSBs of YPIN are the input port, and the lower 16 bits become “don’t cares” if ACC = 00. $YPIN_{31}$ is the MSB.
$RXOUT_{15-0}$	83, 85, 86, 87, 89, 90, 92, 93, 95, 96, 97, 99, 100, 101, 103, 104	D13, D12, C13, B13, C12, A13, B12, A12, B11, A11, B10, A10, B9, A9, B8, A8	$RXOUT_{15-0}$ is the registered Polar Magnitude (Radius) or X-coordinate 16-bit output data port. This output is forced into the high-impedance state when $\overline{OERX}$=HIGH. $RXOUT_{15}$ is the MSB.
$PYOUT_{15-0}$	107, 108, 109, 111, 112, 113, 115, 116, 117, 119, 120, 2, 3, 5, 6, 7	A7, A6, B6, A5, B5, A4, B4, A3, A2, B3, A1, B2, B1, C2, C1, D2	$PYOUT_{15-0}$ is the registered Polar Phase angle or Cartesian Y-coordinate 16-bit output data port. This output is forced to the high-impedance state when $\overline{OEPY}$=HIGH. $PYOUT_{15}$ is the MSB.
Controls			
ENXR	59	M11	The value presented to the input port XRIN is latched into the input registers on the current clock when ENXR is HIGH. When ENXR is LOW, the value stored in the register remains unchanged.
$ENYP_{1,0}$	17, 15	G1, G2	The value presented to the YPIN input port is latched into the phase accumulator input registers on the current clock, as determined by the control inputs $ENYP_{1,0}$, as shown below: **Register Operation** $ENYP_{1,0}$ M C 00 hold hold 01 load hold 10 hold load 11 clear load where C is the Carrier register and M is the Modulation register, and 0=LOW, 1=HIGH. See the Functional Block Diagram.
RTP	11	E1	This registered input selects the current transformation mode of the device. When RTP is HIGH, the TMC2330A executes a Rectangular-To-Polar conversion. When RTP is LOW, a Polar-To-Rectangular conversion will be performed. The input and output ports are then configured to handle data in the appropriate coordinate system. This is a static input. See the Timing Diagram.

Pin Descriptions (continued)

Pin Name	Pin Number		Description
	PPGA	MQFP	
$ACC_{1,0}$	19, 18	H2, H1	In applications utilizing the TMC2330A to perform waveform synthesis and modulation in the Polar-To-Rectangular mode (RTP=LOW), the user determines the internal phase Accumulator structure implemented on the next clock by setting the accumulator control word $ACC_{1,0}$, as shown below: **$ACC_{1,0}$ Configuration** 00 No accumulation performed (normal operation) 01 PM accumulator path enabled 10 FM accumulator path enabled 11 (Nonsensical) logical OR of PM and FM where 0 = L0W, 1 = HIGH. See the Functional Block Diagram. The accumulator will roll over correctly when full-scale is exceeded, allowing the user to perform continuous phase accumulation through 2π radians or 360 degrees. Note that the accumulators will also function when RTP=HIGH (Rectangular-To-Polar), which is useful when performing backward mapping from Cartesian to polar coordinates. However, most applications will require that $ACC_{1,0}$ be set to 00 to avoid accumulating the Cartesian Y input data.
TCXY	14	F1	The format select control sets the numeric format of the Rectangular data, whether input (RTP=HIGH) or output (RTP=LOW). This control indicates two's complement format when TCXY=HIGH and sign-and-magnitude when LOW. This is a static input. See the Timing Diagram.
OVF	105	B7	When RTP=LOW (Polar-To-Rectangular), the Overflow Flag will go HIGH on the clock that the magnitude of either of the current Cartesian coordinate outputs exceeds the maximum range. It will return LOW on the clock that the Cartesian out-put value(s) return to full-scale or less. See the Applications Discussion section. Overflow is not possible in Rectangular-To-Polar mode (RTP = HIGH).
$\overline{OERX}$, $\overline{OEPY}$	81, 9	E13, D1	Data in the output registers are available at the outputs of the device when the respective asynchronous Output Enables are LOW. When $\overline{OERX}$ or $\overline{OEPY}$ is HIGH, the respective output port(s) is in the high impedance state.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		-0.5		7.0	V
Input Voltage		-0.5		V_{DD} + 0.5	V
Output Applied Voltage[2]		-0.5		V_{DD} + 0.5	V
Externally Forced Current[3,4]		-3.0		6.0	V
Short-Circuit Duration	Single output in HIGH state to ground			1	sec
Operating Temperature		-20		110	°C
Ambient Temperature		-20		110	°C
Storage Temperature		-65		150	°C
Junction Temperature			140		°C
Lead Soldering	10 seconds			300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock frequency	TMC2330A			20	MHz
		TMC2330A-1			40	MHz
		TMC2330A-2			50	MHz
t_{PWH}	Clock Pulse Width, HIGH		7			ns
t_{PWL}	Clock Pulse Width, LOW		6			ns
t_S	Input Data Setup Time		6			ns
t_H	Input Data Hold Time		1			ns
V_{IH}	Input Voltage, Logic HIGH		2.0			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Nom	Max	Units
I_{DD}	Power Supply Current	V_{DD} = Max, C_{LOAD} = 25pF, f_{CLK} = Max				
		TMC2330A			140	mA
		TMC2330A-1			240	mA
		TMC2330A-2			290	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, $\overline{OERX}$, $\overline{OEPY}$ = HIGH, f_{CLK} = Max				
		TMC2330A			95	mA
		TMC2330A-1			175	mA
		TMC2330A-2			215	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, CLK = LOW			5	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	S_{15-0}, I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	S_{15-0}, I_{OL} = Max			0.4	V

Switching Characteristics

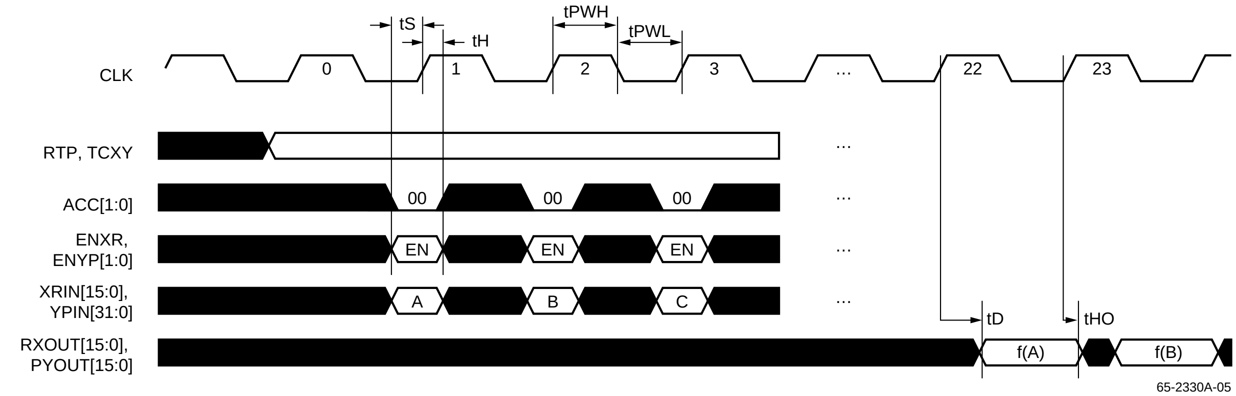
Parameter		Conditions[1]	Min	Nom	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			16	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	3			ns
t_{ENA}	Three-State Output Enable Delay	C_{LOAD} = 0 pF			13	ns
t_{DIS}	Three-State Output Disable Delay	C_{LOAD} = 0 pF			13	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{ENA} and t_{DIS}.

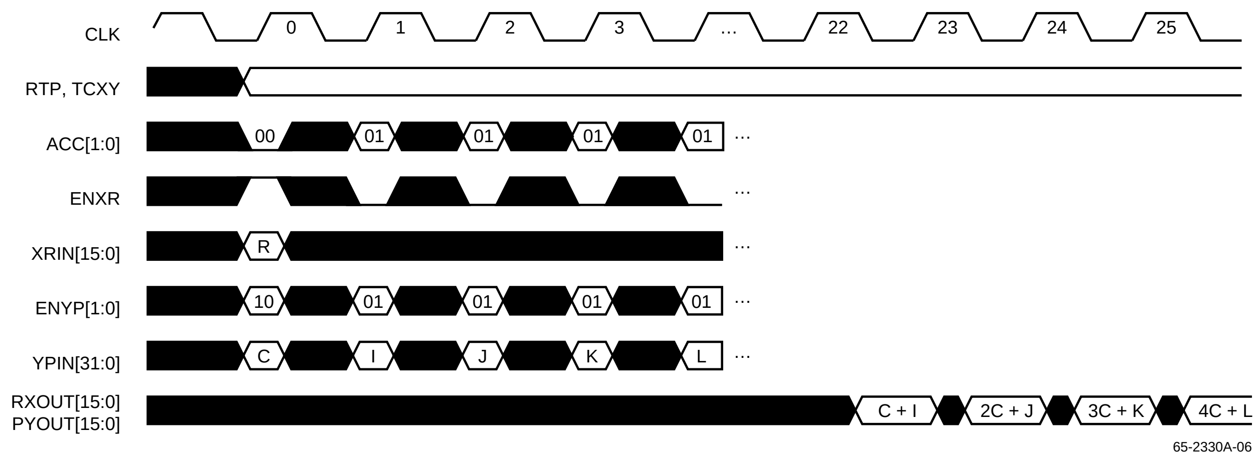
Timing Diagrams

No Accumulation



Note: $\overline{OERX}$ = $\overline{OEPY}$ = LOW

Phase Modulation



Notes:

1. $\overline{OERX}$ = $\overline{OEPY}$ = LOW
2. Carrier C and amplitude R loaded on CLK0.
3. Modulation Values I, J, K, L… Loaded on CLK1, CLK2, etc.
4. Output corresponding to modulation loaded at CLKi emerged tDO after CLKi + 21.
5. To modulate amplitude, vary XRIN with ENXR = 1.

Applications Discussion

Numeric Overflow

Because the TMC2330A accommodates 16-bit unsigned radii and 16-bit signed Cartesian coordinates, Polar-To-Rectangular conversions can overflow for incoming radii greater than 32767= 7FFFh and will overflow for all incoming radii greater than 46341=B505h. (ln signed magnitude mode, a radius of 46340 = B504h will also overflow at all angles.) The regions of overflow and of correct conversion are illustrated in Figure 1.

In signed magnitude mode, overflows are circularly symmetrical—if a given radius overflows at an angle P, it will also overflow at the angles π-P, π+P, and -P. This is because -X will overflow if and only if X overflows, and -Y will overflow if and only if Y overflows.

In two’s complement mode, the number system’s asymmetry complicates the overflow conditions slightly. An input vector with an X component of -32768=8000h will not overflow, whereas one with an X component of +32768 will. Table 3 summarizes several simple cases of overflow and near-overflow.

Table 3a. X-Dimensional Marginal Overflows

TC	YPIN	OV	RXOUT	CORRECT X
0	0000 = 0	1	0000 = +0	+32768
0	8000 = π	1	8000 = -0	-32768
1	0000 = 0	1	8000 = -32768	+32768
1	8000 = π	0	8000 = -32768	-32768

In all cases, RTP=0 (Polar-To-Rectangular mode) and XRIN=8000 (incoming radius=32768).

Table 3b. Maximal Overflow (Radius In=65535)

TC	YPIN	OV	RXOUT	CORRECT X
0	0000 = 0	1	7FFF = +32767	+65535
0	8000 = π	1	FFFF = -32767	-65535
1	0000 = 0	1	FFFF = -1	+65535
1	8000 = π	1	0001 = +1	-65535

In all cases, RTP=0 (Polar-To-Rectangular mode) and XRIN=7FFF (incoming radius=65535, which will always overflow).

Numeric Underflow

In RTP=1 (Rectangular-To-Polar) mode, if XRIN=YPIN=0, the angle is undefined. Under these conditions, the TMC2330A will output the expected radius of 0 (RXOUT= 0000) and an angle of 1.744 radians (PYOUT=4707). This angle is an artifact of the CORDIC algorithm and is not flagged as an error, since the angle of any 0 length vector is arbitrary.

Performing Scan Conversion with the TMC2330A

Medical Imaging Systems such as Ultrasound, MRI, and PET, and phased array Radar and Sonar systems generate radial-format coordinates (range or distance, and bearing) which must be converted into raster-scan format for further processing and display. Utilizing the TMC2302 Image Resampling Sequencer, a minimum chipcount Scan Converter can be implemented which utilizes the trigonometric translation performed by the TMC2330A to backwards-map from a Cartesian coordinate set into the Polar source image buffer address space.

As shown in Figure 2, the TMC2330A transforms the Cartesian source image addresses from the TMC2302 directly to vector distance and angle coordinates, while the TMC2302 writes the resulting resampled pixel values into the target memory in raster fashion. Note that the ability to perform this spatial transformation in either direction gives the user the freedom to process images in either coordinate space, with little restriction. Image manipulation such as zooms or tilts can easily be included in the transformation by programming the desired image manipulation into the TMC2302's transformation parameter registers.

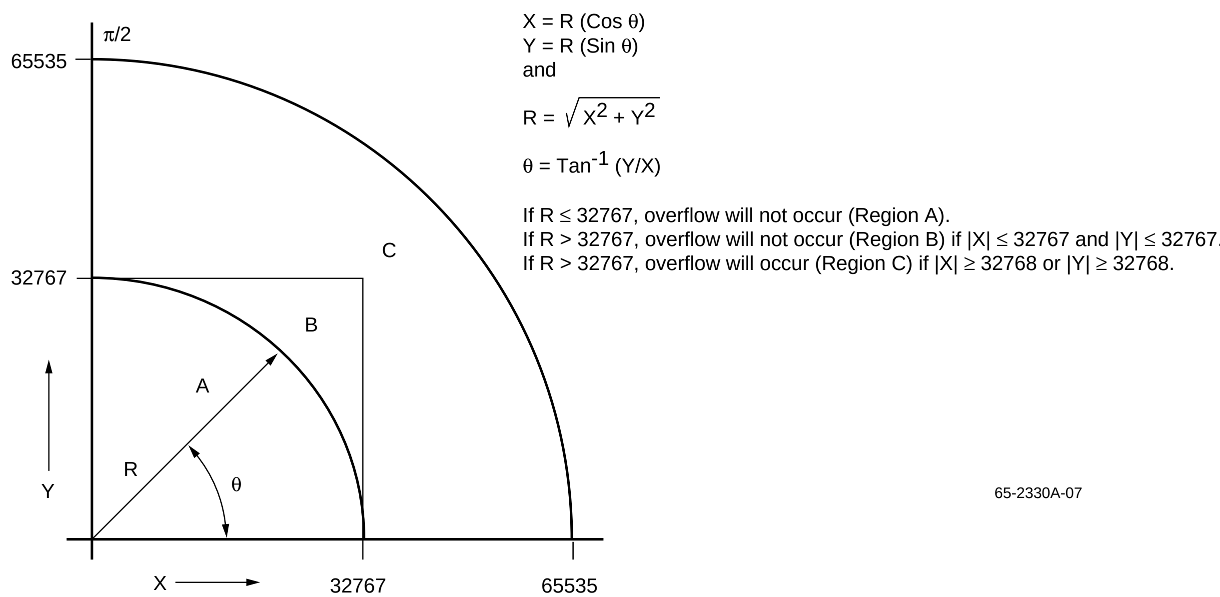


Figure 1. First Quadrant Coordinate Relationships

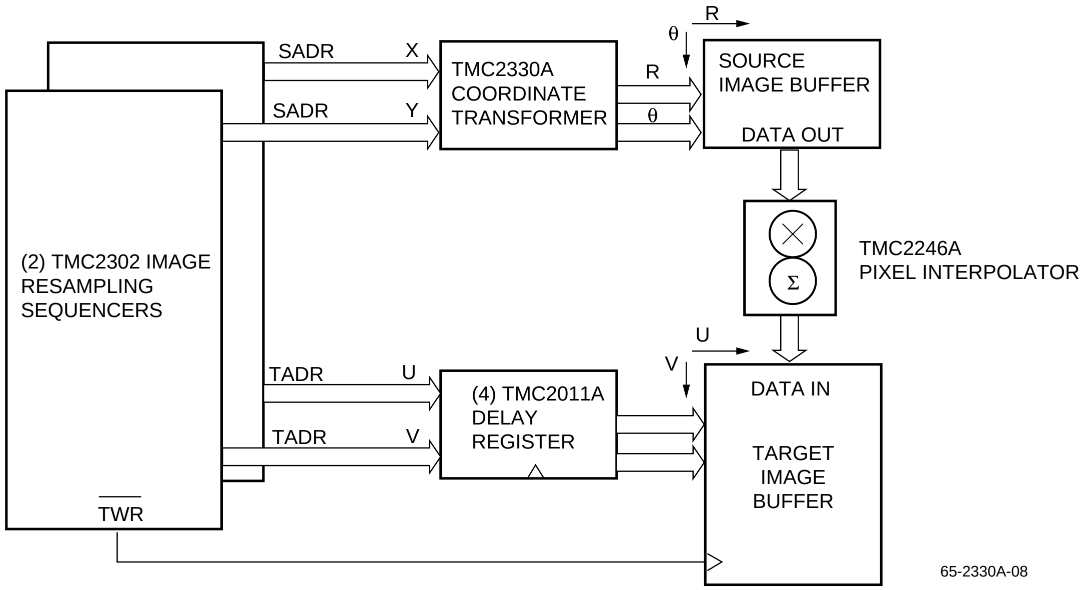


Figure 2. Block Diagram of Scan Converter Circuit Utilizing TMC2330A and TMC2302 Image Resampling Sequencer

Arithmetic Error for Two's Complement Rectangular to Polar Conversion

A random set of 5000 input vector coordinate pairs (X,Y), uniformly spread over a circle of radius 32767 was converted to polar coordinates.

Radius Error Range	–0.609 to 0.746 LSB
Mean Radius Error	0.019 LSB
Mean Absolute Radius Error	0.252 LSB
Phase Error Range	–1.373 to 1.469 LSB
Mean Phase Error	0.058 LSB
Mean Absolute Phase Error	0.428 LSB

Statistical Evaluation of Double Conversion

In this empirical test, 10,000 random Cartesian vectors were converted to and from polar format by the TMC2330A. The resulting Cartesian pairs were then compared against the original ones. The un-restricted database represents uniform sampling over a square bounded by -32769<x<32768 and -32769<y<32768.

The results of the 10,000-vector study were as follows:

Mean Error (X)	+0.0052 LSB
Mean Error (Y)	0.0031 LSB
Mean Absolute Error (X)	0.662 LSB
Mean Absolute Error (Y)	0.664 LSB
Root Mean Square Error (X)	1.025 LSB
Root Mean Square Error (Y)	1.020 LSB
Max Error (X)	+4/ -5 LSB
Max Error (Y)	+5 -4 LSB

Since this is a double conversion (rectangular to polar and back) which includes a wide variety of "good case" and "bad case" vectors, the chip should perform even better in many real systems. Repeating the experiment and restricting the original data set to an annulus defined by 8196<R<32768 reduced the mean square error to 0.89 LSB and the peak error to ±4 LSB (x or y). These latter results are more germane to synthesizer, demodulator, and other applications in which the amplitude can be restricted to lie between quarter and full scale. The largest errors tend to occur in the angle component of small radius cartesian-to-polar conversion.

Equivalent Circuits

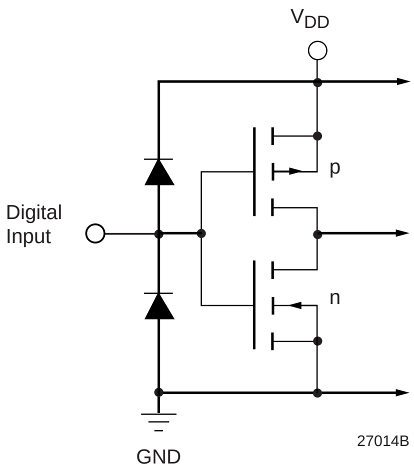


Figure 3. Equivalent Input Circuit

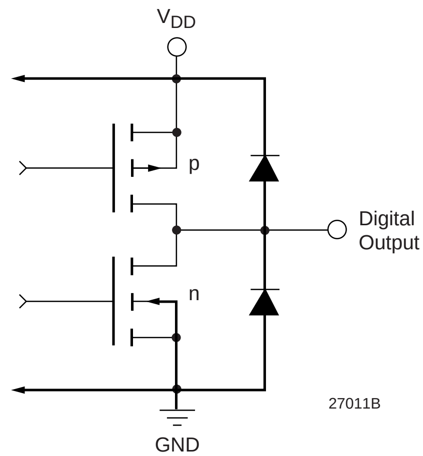


Figure 4. Equivalent Output Circuit

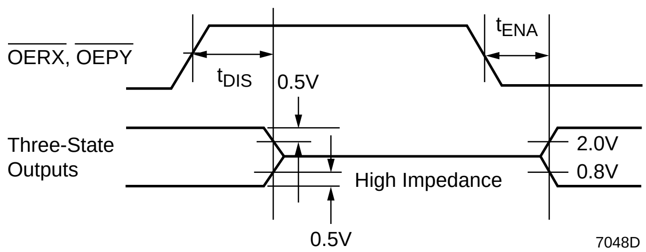


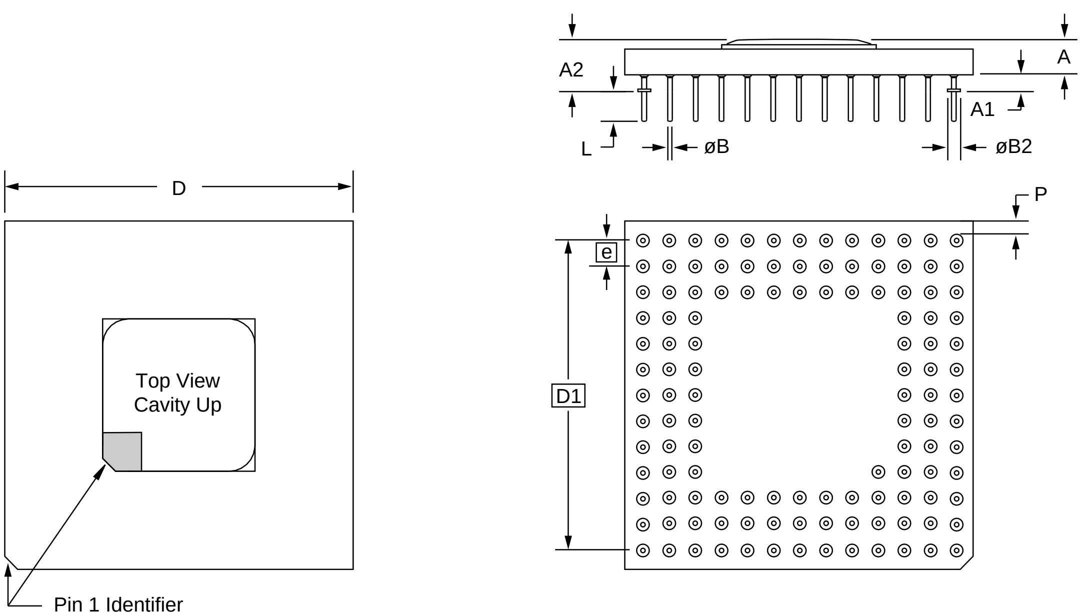
Figure 5. Transition Levels for Three-State Measurements

Mechanical Dimensions

121-Lead PPGA Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.340	1.380	33.27	35.05	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
L1	.170	.190	4.31	4.83	
M	13		13		3
N	120		120		4
P	.003	—	.076	—	

Notes:
1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



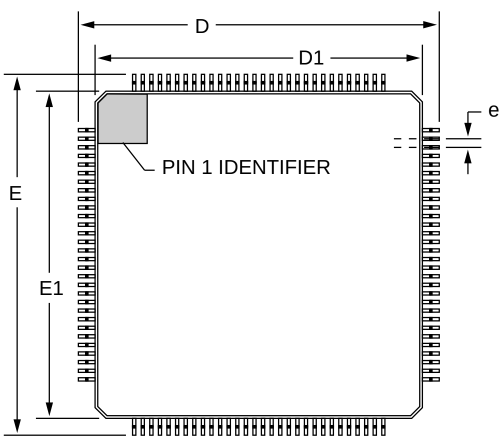
Mechanical Dimensions (continued)

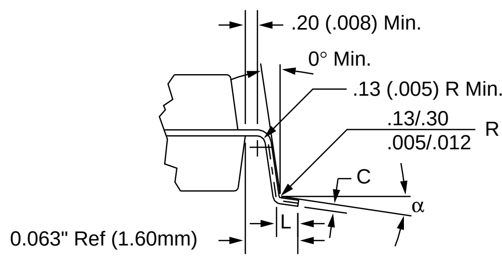
120-Pin MQFP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.154	—	3.92	
A1	.010	—	.25	—	
A2	.125	.144	3.17	3.67	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D/E	1.219	1.238	30.95	31.45	
D1/E1	1.098	1.106	27.90	28.10	
e	.0315 BSC		.80 BSC		
L	.026	.037	.65	.95	4
N	120		120		
ND	30		30		
α	0°	7°	0°	7°	
ccc	—	.004	—	.10	

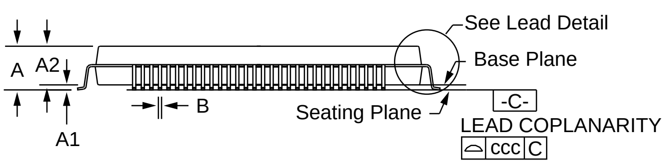
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail



Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2330AH5C	0° to 70°C	20 MHz	Commercial	120-Pin Plastic Pin Grid Array	2330AH5C
TMC2330AH5C1	0° to 70°C	40 MHz	Commercial	120-Pin Plastic Pin Grid Array	2330AH5C1
TMC2330AH5C2	0° to 70°C	50 MHz	Commercial	120-Pin Plastic Pin Grid Array	2330AH5C2
TMC2330AKEC	0° to 70°C	20 MHz	Commercial	120-Pin Metric Quad FlatPack	2330AKEC
TMC2330AKEC1	0° to 70°C	40 MHz	Commercial	120-Pin Metric Quad FlatPack	2330AKEC1
TMC2330AKEC2	0° to 70°C	50 MHz	Commercial	120-Pin Metric Quad FlatPack	2330AKEC2

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